REMARKS

The Applicants would like to thank the Examiner for the thorough examination of the present application. In view of the supporting arguments presented in detail below, it is submitted that all of the claims are patentable.

I. The Claimed Invention

The present invention is directed to a computer system. As recited in independent Claim 5, for example, the computer system includes a master apparatus and a slave apparatus for communicating asynchronously therewith via a universal serial bus (USB) protocol. The slave apparatus includes a sending/receiving circuit for sending and receiving binary information to and from the master apparatus and supplying status signals based thereon. Moreover, a plurality of state latches and control circuitry cooperating therewith receive the status signals from the sending/receiving circuit and supply state signals of the sending/receiving circuit based thereon.

The slave apparatus further includes a microprocessor for processing applications of the slave apparatus and also for processing the binary information received by the sending/receiving circuit when an interruption signal is supplied. Furthermore, an interruption state latch and a control circuit cooperating therewith supply the interruption signal to the microprocessor once the start of a new message from the master apparatus has been acknowledged and recorded by the sending/receiving circuit. The sending/receiving circuit also acknowledges the start of a

following message from the master apparatus while the interrupt signal is supplied.

The microprocessor advantageously allows the slave apparatus, at the end of a message, to accept the start of a following message while the microcontroller is unavailable. That is, the computer system addresses the problem of receiving the first part of a new message while the microprocessor is not available.

Independent Claim 11 is directed to a similar computer system, and independent Claim 17 is directed to a related slave apparatus. Independent Claim 20 is directed to a related method.

II. The Claims Are Patentable

The Examiner rejected independent Claims 5, 11, 17, and 20 over the "admitted prior art" in view of Lee. The admitted prior art describes a typical master-slave computer system arrangement, such as the one illustrated in FIG. 1 of the present application.

Beginning on page 2, line 29, it is noted that during different transfer stages between the master apparatus and the slave apparatus, there are provisions which allow the master apparatus to repeat its part of the message IN and OUT while the microcontroller (i.e., microprocessor) of the slave apparatus is unavailable. If the phase that follows is a start phase and its microcontroller is unavailable, the slave apparatus returns no signal (no NAK, nor STALL, nor ACK signal), which is interpreted by the master apparatus as a transmission error. In such case the master apparatus resends the message.

In other words, the master apparatus does not allow the slave apparatus, at the end of a message, to accept the start of a following message while the microcontroller of the salve apparatus is unavailable. The Examiner correctly acknowledges that the admitted prior art fails to teach or fairly suggest that 1) the microcontroller processes the binary information received by the sending receiving circuit when the interruption signal is supplied; 2) the interruption signal is supplied once the start of a new message has been acknowledged and recorded by the sending/receiving circuit; and 3) the sending/receiving circuit also acknowledges the start of a following message while the interruption signal is supplied.

The Examiner contends that Lee properly supplies these noted deficiencies. Lee is directed to a method and apparatus for providing reliable interrupt reception over a buffered bus by utilizing a mailbox register to receive interrupt request information sent after a data write transaction. The Applicants respectfully submit that although the host acts as a slave device in Lee, the latter is still very different from a universal serial bus (USB) configuration. Namely, Lee's configuration involves several master devices sending data packets to the slave device (i.e., the host), which should handle all the packets received.

As readily appreciated by those skilled in the art, a USB configuration includes a single master device that can selectively send data packets to several slave devices. To this end, each data packet contains an identifier allowing each slave device to determine whether or not it should accept the subsequent data. Lee's system allows handling of several

data packets which may come from different sources, which are stored in a buffered bus, and which may arrive at any time to the host. Thus, the objective of Lee is clearly to be able to receive and handle all the data without any restriction on the time they arrive.

The USB protocol allows a slave device to refuse a packet when it is not ready to handle such a packet, in which case the refused packet is sent again by the host after a certain delay. However, this general rule has an exception, which is the case of a "SETUP" packet. A "SETUP" packet is a particular packet initiating a sequence of transactions, and should always be accepted by the slave device to comply with the USB protocol.

A problem addressed by the invention arises from the fact that the host may decide to send a second setup packet at any time, while the slave is supposed to reject any data packet as long as the data processing entailed by a setup packet (execution of the CTR interrupt) is not completed.

In the case of a second "SETUP" packet being sent to the slave while the processing entailed by receipt of the first setup packet is not finished yet, the first packet is overwritten by the second one, and the processor is informed to this situation so that the handling of this packet should be resumed (SOVR flag).

The Applicants thus submit that since the Lee patent is not directed to a USB configuration, there is no motivation to selectively modify the "admitted prior art" in view of Lee as suggested by the Examiner. Lee's system allows handling of several data packets which may come from different sources, which are stored in a buffered bus, and which may arrive at

any time to the host. Thus, the objective of Lee is to be able to receive and handle all the data without any restriction on the time they arrive.

In the claimed invention, the USB configuration includes a master device that can selectively send data packets to the slave device. To this end, the microcontroller processes the binary information received by the sending receiving circuit when the interruption signal is supplied; the interruption signal is supplied once the start of a new message has been acknowledged and recorded by the sending/receiving circuit; and the sending/receiving circuit also acknowledges the start of a following message while the interruption signal is supplied.

Accordingly, it is submitted that independent Claim 5 is patentable over the "admitted prior art" in view of Lee. Independent Claims 11, 17, and 20 are similar to independent Claim 5. Therefore, it is submitted that these claims are also patentable over the "admitted prior art" in view of Lee.

In view of the patentability of independent Claims 5, 11, 17 and 20, it is submitted that the dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

III. CONCLUSION

In view of the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the

telephone number listed below.

Respectfully submitted,

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